

What Is Claimed Is:

1 1. A input/output buffer protection circuit,
2 comprising:

3 an I/O pad;

4 an I/O buffer, comprising a first PMOS transistor and a
5 first NMOS transistor;

6 an n-well control circuit coupled to an n-well of the first
7 PMOS transistor and the I/O pad for raising the n-well
8 of the first PMOS transistor to a input voltage level
9 when the input voltage is greater than a source
10 voltage;

11 a gate control circuit coupled to a gate terminal of the
12 first PMOS transistor and the n-well control circuit
13 for raising the gate terminal of the PMOS transistor
14 to the input voltage level when the input voltage
15 is greater than the source voltage, the gate control
16 circuit comprises a transistor for passing a control
17 voltage to the gate of the PMOS transistor in output
18 mode; and

19 wherein the n-well control circuit comprising a protection
20 component, providing a voltage drop down path from
21 the gate of the transistor to the I/O pad and block
22 the I/O pad signal flow back to the gate of the
23 transistor.

1 2. The input/output buffer protection circuit of claim
2 1, wherein the N-Well control circuit comprising:

3 a second PMOS transistor, wherein the gate terminal of the
4 second PMOS is connected to a source voltage V_{cc} , a

5 source terminal of the second PMOS is connected to
6 the I/O pad, and the drain terminal of the second PMOS
7 is connected to the n-well of the PMOS transistor of
8 the I/O buffer;and
9 a third PMOS transistor, wherein the gate terminal of the
10 third PMOS is connected to a source voltage, a source
11 terminal of the third PMOS is coupled to the I/O pad,
12 a n-well of the third PMOS is connected to the drain
13 terminal of the second PMOS; and
14 a fourth PMOS transistor, wherein the gate terminal of the
15 fourth PMOS transistor is connected to the drain of
16 the third PMOS, a source terminal is connected to the
17 source voltage, and the drain terminal of the fourth
18 PMOS is connected to the n-well of the third PMOS.

1 3 The input/output buffer protection circuit of claim
2 2, wherein the transistor of the gate control circuit is a sixth
3 PMOS transistor, the gate control circuit further comprising:
4 a fifth PMOS transistor,
5 wherein the gate terminal of the fifth PMOS is connected
6 to the source voltage, the source terminal is
7 connected to the I/O pad ;
8 a sixth PMOS transistor, wherein the gate terminal is
9 connected to the drain of the third PMOS, a source
10 terminal is connected to the control signal, and a
11 drain terminal coupled to the gate of the first PMOS;
12 and
13 a second NMOS transistor, wherein a gate terminal of the
14 NMOS is connected to the source voltage, a drain
15 terminal is connected to the control signal, and a

16 source terminal is connected to the gate of the first
17 PMOS.

1 4. The input/output buffer protection circuit of claim
2 1 or claim 3, wherein the protection component is an NMOS
3 transistor.

1 5. The input/output buffer protection circuit of claim
2 4, wherein a gate terminal and a source terminal are coupled to
3 a node A which is connected to the gate of the sixth PMOS
4 transistor, a drain terminal of the NMOS transistor is connected
5 to the I/O pad.

1 6. The input/output buffer protection circuit of claim
2 1, wherein the protection component is a PMOS transistor.

1 7. The input/output buffer protection circuit of claim
2 1, wherein the protection component is a diode configured
3 device.